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[Chao Wang, Frank Mueller, Christian Engelmann, Stephen L. Scott](#)  
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As the number of nodes in high-performance computing environments increases, hardware faults are becoming common place. Reactive fault tolerance (FT) often cannot cope due to massive I/O requirements and relies on manual job resubmission or

- 2 [Proactive fault tolerance for HPC with Xen virtualization](#)  
[Arun Babu Nagarajan, Frank Mueller, Christian Engelmann, Stephen L. Scott](#)  
 June 2007 ICS '07: Proceedings of the 21st annual international conference on Supercomputing  
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Large-scale parallel computing is relying increasingly on clusters with thousands of processors. At such large counts of compute nodes, faults are becoming common. Current techniques to tolerate faults focus on reactive schemes to recover

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[Ronny Krashinsky, Christopher Batten, Krste Asanović](#)  
 July 2008 Transactions on Design Automation of Electronic Systems  
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 Publisher: ACM  
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The Scale vector-thread processor is a complexity-effective solution for computing which flexibly supports both vector and highly multithreaded workloads. The 7.1-million transistor chip has 16 decoupled execution clusters, vector processors, and a hybrid C++/Verilog simulation, iterative

Keywords: Vector processors, hybrid C++/Verilog simulation, iterative


flow, multithreaded processors, procedural datapath pre-placement, ver  
processors

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 Michael Schiassner, Nagabhushan Chittur, Erwin Oertli, Paul M. Stillwell, Jr  
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 Jaejin Lee, Junghyun Kim, Choonki Jang, Seungkyun Kim, Bernhard Egger,  
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There have been strong demands for a fast and cycle-accurate virtual p  
 embedded systems area where developers can do meaningful software  
 including performance debugging in the context of the entire platform. I





Keyw ords: architecture simulator, cycle-accurate simulation, full-syste  
 simulator parallelization, virtual prototyping

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